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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,349	12/23/2003	Bryan K. Casper	INTEL-0064	4699

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EXAMINER	
WALLING, MEAGAN S	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/743,349	CASPER ET AL.	
	Examiner	Art Unit	
	Meagan S. Walling	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17,19,20,22-24 and 26-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *31-34* is/are allowed.

6)☒ Claim(s) *1,5,8-11,15,16,19,20,26,27,29 and 30* is/are rejected.

7)☒ Claim(s) *2-4,6,7,12-14,17,22-24 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/23/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 5, 8, 11, 15, 16, 20, 26, and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Shimoda (US 5,373,257).

Regarding claim 1, Shimoda teaches a first port to receive a first signal from a first channel (Fig. 2, input signal); a first device, coupled to the first port, to modify a channel response of the first signal received from the first channel, the first device including a filtering device (13) having a plurality of voltage-to-current converters (14, 15) and a plurality of current multipliers coupled in a plurality of stages (column 2, lines 34-36); and a waveform capture device, coupled to the first device, to capture a waveform of a signal modified by the first device (11).

Regarding claim 5, Shimoda teaches a second port to receive a second signal form a second channel (Fig. 9, input signal); a second device, coupled to the second port, to modify a channel response of the second signal received from the second channel (12); and another waveform capture device, coupled to the second device, to capture a waveform of a signal modified by the second device (33).

Regarding claim 8, Shimoda teaches that each of the plurality of stages provides a separate response (column 5, lines 49-57).

Regarding claim 11, Shimoda teaches a processing circuit to receive a signal across a channel and perform signal processing on the signal, the processing circuit including a filtering circuit coupled in a plurality of stages (13), each of the stages to provide a separate response, the processing circuit to output a processes signal based on the separate responses (column 5, lines 49-57); and a waveform capture device to capture a waveform of the signal based on the processed signal (11).

Regarding claim 15, Shimoda teaches that the processing circuit modifies a channel response of the received signal (column 5, lines 49-57).

Regarding claim 16, Shimoda teaches that the filtering circuit includes a plurality of voltage-to-current converters (14, 15) and a plurality of current multipliers (column 2, lines 34-36).

Regarding claim 20, Shimoda teaches receiving a signal (Fig. 2, input signal) from a channel; modifying a channel response of the received signal by performing a filtering operation on the received signal, the filtering operation including dividing the received signal into a plurality of stages, each stage providing a separate response (Ref. 13 and column 5, lines 49-57); and capturing a waveform of a signal having a modified channel response (see Ref. 11).

Regarding claim 26, Shimoda teaches that each of the stages includes a voltage-to-current converter and a current multiplier (column 2, lines 34-36).

Regarding claim 27, Shimoda teaches that the filtering operation further includes combined filtered responses (Ref. 13, 14, 15 and column 2, lines 34-36).

2. Claims 9, 10, 19, 29, and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Bowers et al. (US 5,648,735).

Regarding claim 9, Bowers et al. teaches a first port to receive a first signal from a first channel (see Fig. 3); a first device, coupled to the first port, to modify a channel response of the first signal received form the first channel (22); and a waveform capture device, coupled to the first device, to capture a waveform of a signal modified by the first device, the waveform capture device including a variable offset to skew a reference current (Ref. 26 and column 5, lines 12-14).

Regarding claim 10, Bowers et al. teaches that the signal comprises a differential signal (22).

Regarding claim 19, Bowers et al. teaches a processing circuit to receive a signal across a channel and perform signal processing on the signal, the processing circuit to output a processed signal (22); and a waveform capturing device to capture a waveform of the signal based on the processed signal, the waveform capturing device including a variable offset to skew a reference circuit (Ref. 26 and column 5, lines 12-14).

Regarding claim 29, Bowers et al. teaches receiving a signal from a channel (column 5, lines 9-10); modifying a channel response of the received signal (column 5, lines 10-12); and capturing a waveform of a signal having the modified channel response by skewing a reference current (column 5, lines 12-14).

Regarding claim 30, Bowers et al. teaches receiving another signal across another channel (column 5, line 8); modifying a channel response of the received another channel

(column 5, lines 10-12); and capturing a waveform of a signal having the modified channel response (column 5, lines 12-14).

Allowable Subject Matter

3. Claims 2-4, 6-7, 12-14, 17, 22-24, and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The primary reason for the indication of allowability of claims 2, 12 is the inclusion of the limitation that the first device further includes a sampling circuit. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 6 is the inclusion of the limitation that the second device comprises a filtering device that includes a plurality of voltage-to-current converters and a plurality of current multipliers coupled in a plurality of stages. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 7 is the inclusion of the limitation that the filtering device further includes a plurality of sampling circuits to sample the signal received at the first port. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 17 is the inclusion of the limitation that the filtering circuit further includes a plurality of sampling circuits to sample the

received signal. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

The primary reason for the indication.of allowability of claim 22 is the inclusion of the limitation of a sampling operation of the received signal. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

The primary reason for the indication of allowability of claim 28 is the inclusion of the limitation of sampling the combined filtered response. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

4. Claims 31-34 are allowed.

The following is an examiner's statement of reasons for allowance:

The primary reason for the allowance of claim 31 is the inclusion of the limitation of an integrated circuit including a port to receive a signal from a channel, a processing device, coupled to the port, to modify a channel response of the signal received from the channel, and a waveform device, coupled to the processing device, to capture a waveform of a signal modified by the processing device, the processing device including a filtering device having a plurality of voltage-to-current converters and a plurality of current multipliers coupled in a plurality of stages; and a network interface to couple the integrated circuit to a network. It is this limitation in the claimed combination that has not been found, taught, or suggested by the prior art that makes these claims allowable.

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Meagan S. Walling whose telephone number is (571) 272-2283. The examiner can normally be reached on Monday through Friday 8:30 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

msw

BRYAN BUI
PRIMARY EXAMINER